

Short Course on Selected Topics in Data Converter Design

By **Boris Murmann** and **Paul Jespers**

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Venue: University of Limerick



UNIVERSITY of LIMERICK

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This course will cover advanced topics related to integrated CMOS circuit design for data converters. Focus is placed on topics that haven't received an up-to-date treatment in commonly used textbooks. The specific subjects include fundamentals (design of samplers and comparators, noise analysis) as well as advanced material on the design of SAR ADCs and time interleaved architectures.

The afternoon of the second day is devoted to g_m/I_D -based sizing, and is a re-run of a tutorial that will be presented at ISCAS 2015: "Systematic Design of Analog Circuits Using Pre-Computed Lookup Tables." The outline is appended below.

Monday, 17th August, 2015

08:30-10:00 Sampling circuits
10:30-12:00 Voltage comparators
01:30-03:00 Noise analysis and simulation in SC circuits
03:30-05:00 SAR ADCs

Tuesday, 18th August, 2015

08:30-10:00 Aspects of time-interleaved ADC design
10:30-12:00 Data converter performance trends
ISCAS Tutorial on g_m/I_D -based Design (with Paul Jespers):
01:30-03:00 Part I
03:30-05:00 Part II

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Abstract of Tutorial on g_m/I_D -based Design

Systematic Design of Analog Circuits Using Pre-Computed Lookup Tables

The majority of textbook material on analog circuit design is based on the square-law model for MOS transistors. While this model remains useful for teaching, it has become too inaccurate for design in nano-scale CMOS. In circuit simulators, this problem has been solved using complex models equations with hundreds of parameters. Since these descriptions are impractical for manual use, designers tend to shy away from hand-analysis-based optimization and resort to a design style built on iterative and time-consuming “tweaking” in a simulator.

This tutorial presents a systematic design methodology that bridges the gap between simulation, hand analysis and script-based optimization. The approach hinges upon Spice-generated look-up tables containing the transistor’s equivalent model parameters (g_m , g_{ds} , etc.) across a multi-dimensional sweep of the terminal voltages. We interpret and organize these data based on the transistor’s inversion level, employing g_m/I_D as a proxy and key parameter for design. This width-independent metric captures a device’s efficiency in translating bias current to transconductance and spans nearly the same range in all modern CMOS processes ($\sim 3 \dots 30$ S/A). When combined with other width-independent figures of merit (g_m/C_{gg} , g_m/g_{ds} , etc.) thinking in terms of g_m/I_D (rather than gate overdrive) allows us to study the tradeoffs between bandwidth, noise, distortion and power dissipation in a normalized space. The final bias currents and device sizes follow from a straightforward de-normalization step using the current density I_D/W . Since this entire flow is driven by Spice-generated data, we maintain close agreement between the desired specs and the circuit’s simulated performance.

Our tutorial will detail the inner workings of this approach, and showcase its capabilities using a variety of practical examples. These will include the design of low-noise and low-distortion gain stages, operational amplifiers, voltage regulators, etc. In addition, we will present suitable flows for the inclusion of process corners.

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Biographies

Paul Jespers received the Electrical and Civil Engineer degree from the Université Libre de Bruxelles (ULB) in 1953 and the Doctorate in Applied Sciences from the Université Catholique de Louvain (UCL), Be, in 1959. He started working in the domain of radio interference instrumentation. He joined the Electrical Department of Applied Sciences Faculty of the UCL in 1959, where he started the Microelectronics Laboratory mid 60's. Visiting Professor at Universities in France, Italy, Spain, U.S.A, Latin America, Australia, China and India where he was appointed UNIDO expert. Prof. Jespers is an IEEE Fellow, Doctor Honoris Causa from U.C. Cordoba University (Argentina) and F.P.Ms (Belgium). He is now Emeritus Professor of UCL. Prof Jespers contributed to several startup electronic industries in the Belgium.

Boris Murmann joined Stanford University in 2004, where he currently serves as an Associate Professor of Electrical Engineering. He received the Ph.D. degree in electrical engineering from the University of California at Berkeley in 2003. From 1994 to 1997, he was with Neutron Microelectronics, Germany, where he developed low-power and smart-power ASICs in automotive CMOS technology. Dr. Murmann's research interests are in the area of mixed-signal integrated circuit design, with special emphasis on data converters and sensor interfaces. In 2008, he was a co-recipient of the Best Student Paper Award at the VLSI Circuits Symposium in 2008 and a recipient of the Best Invited Paper Award at the IEEE Custom Integrated Circuits Conference (CICC). He received the Agilent Early Career Professor Award in 2009 and the Friedrich Wilhelm Bessel Research Award in 2012. He has served as an Associate Editor of the IEEE Journal of Solid-State Circuits and as the Data Converter Subcommittee Chair of the IEEE International Solid-State Circuits Conference (ISSCC). He currently serves as the program vice-chair for the ISSCC 2016. He is a Fellow of the IEEE.