Online Short-Course on Advanced Data Converter IC Design

By Mike Shuo-Wei Chen

Dates: 4th/6th/10th/13th/17th/20th/24th/27th May 2021

Host: Live Zoom Lectures Hosted by University of Limerick

Course Outline

This course will cover advanced topics in integrated circuit design for data converters with particular focus on low-power SAR ADCs and high-speed DACs on scaled technologies.

Fundamental concepts (sampling, comparators, noise analysis) will be reviewed in depth as well as advanced design techniques used for these specific types of data converters.

The course follows a top-down approach by starting with an overview of the SAR ADC architecture including circuit implementations and error-correction schemes. This is followed by an in-depth discussion of speed enhancement techniques including the asynchronous SAR approach and hybrid architectures based on the SAR topology. We will examine the design of the main building blocks of a SAR ADC: Sampling Network, DAC & Comparator.

An emerging trend of achieving high-speed SAR is via time-interleaving topology. Therefore, we will discuss the key design considerations of time-interleaved SAR, including error mechanisms, calibration schemes and cover state-of-the-art design examples.

Alternative SAR ADC schemes are also presented including the time-based approach and the promising non-uniform sampling ADC. These are emerging ADC architectures for the next generation of data converter design.

The final two sessions of the course will cover in depth the design of high-speed DACs with a review of state-of-the-art design techniques and examples including a dual-rate hybrid DAC architecture that has recently proven to achieve high speed and high linearity.

Course Duration: **16 hrs**

Course Format: **8 'Live' Sessions (2 sessions/wk) x 2 hrs/ea. (90min lecture + 30min Q&A)**

Course Work: **Optional homework sheets & solutions will be distributed via email**

For registration, please contact Hooman Reyhani: hooman.reyhani@ul.ie

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Course Programme

All Lectures @ 16:00-18:00 WET = 17:00-19:00 CET

20:30-22:30 IST = 11:00-13:00 EST = 08:00-10:00 PST

Lecture #1 - SAR ADC – Architecture Design — **4th May 2021**

Architectures, Circuit Implementations, Redundancy Schemes, Calibration Techniques

Lecture #2 - SAR ADC – Speed Enhancement Techniques — **6th May 2021**

Asynchronous SAR, More speed enhancement techniques, Hybrid architectures based on SAR

Lecture #3 - Sampling Network & DAC Design — **10th May 2021**

Implementation considerations, Noise, Jitter, Distortion, Linearity, Design techniques and examples

Lecture #4 - Comparator Design — **13th May 2021**

Implementation considerations, Speed optimization, Noise, Offset, Metastability, Design examples

Lecture #5 – Time-Interleaving — **17th May 2021**

Design consideration, Error mechanisms, Calibration Techniques, Design techniques and examples

Lecture #6 - Time-based/Non-uniform Sampling ADC — **20th May 2021**

Architectures, Design considerations, Circuit implementations, Non-uniform sampling ADC

Lecture #7 - High-Speed DACs – Part I — **24th May 2021**

DAC Specifications, DAC Architectures, Matching requirements, Design techniques and examples

Lecture #8 - High-Speed DACs – Part II — **27th May 2021**

Non-idealities, Calibration Techniques, State-of-the-art Design Examples, Dual-Rate Hybrid DAC

WET = Western European Time, CET = Central European Time,
IST = India Standard Time, EST = Eastern Standard Time, PST = Pacific Standard Time

Mike Shuo-Wei Chen received the B.S. degree from National Taiwan University, Taipei, Taiwan, in 1998 and the M.S. and Ph.D. degree from University of California, Berkeley, in 2002 and 2006, all in electrical engineering. He is a Professor in Electrical Engineering Department at University of Southern California (USC) and holds Colleen and Roberto Padovani Early Career Chair position.

As a graduate student researcher, he proposed and demonstrated the asynchronous SAR ADC architecture, which has been adopted today for low-power high-speed analog-to-digital conversion products in industry. After joining USC, he leads an analog mixed-signal circuit group, focusing on high-speed low-power data converters, bio-inspired/biomedical electronics, RF frequency synthesizers, DSP-enabled analog circuits and systems. His research group has been exploring new circuit architectures that excel beyond the technology limitation, as exemplified in their recent works in PA, ADC, DAC, and PLL. From 2006 to 2010, he has been a member of Analog IC Group at Atheros Communications (now Qualcomm), working on mixed-signal and RF circuits for various wireless communication products.

Dr. Chen was the recipient of NSF Faculty Early Career Development (CAREER) Award, DARPA Young Faculty Award (YFA) both in 2014, Analog Devices Outstanding Student Award for recognition in IC design in 2006 and UC Regents' Fellowship at Berkeley in 2000. He also achieved an honourable mention in the Asian Pacific Mathematics Olympiad, 1994. In terms of services, Dr. Chen has been serving as an associate editor of IEEE Solid-State Circuits Letters (SSC-L), IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II), as well as a TPC member of conferences in IEEE Solid-State Circuits Society, such as IEEE International Solid State Circuits Conference (ISSCC), IEEE VLSI Circuits Symposium, and IEEE Custom Integrated Circuits Conference (CICC).

Past IC Design Courses Arranged by UL-CSRC

400+ participants from Italy, Spain, Portugal, Czech Rep., Switzerland, Romania, India, US, UK & Ireland

2015 Course: Prof. Murmann & Prof. Jespers

IEEE SSC Magazine - Winter 2016

2016 Course: Prof. Murmann

IEEE SSC Magazine - Fall 2016

2017 Course: Prof. Murmann

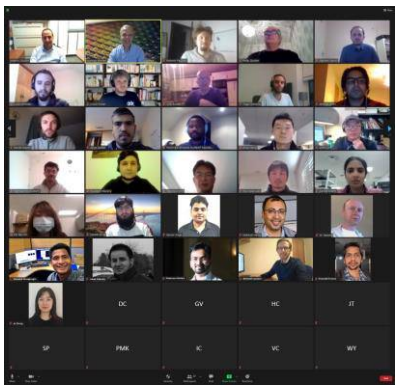
IEEE SSC Magazine - Winter 2018

2018 Course: Prof. Bult

IEEE SSC Magazine - Fall 2018

2019 Course: Prof. Johns

IEEE SSC Magazine - Winter 2020



2020 Course: Prof. Liscidini

IEEE SSC Magazine, Spring 2021 (To Appear)