



# **Online Short-Course on Advanced Wireless Transceiver IC Design**

## By Antonio Liscidini

Dates: 5<sup>th</sup>/12<sup>th</sup>/19<sup>th</sup>/26<sup>th</sup> October & 2<sup>nd</sup>/9<sup>th</sup>/16<sup>th</sup>/23<sup>rd</sup> November 2020

Host: Webinars Hosted by University of Limerick

#### **Course Outline**

This course addresses some of the most recent wireless transceiver circuit design techniques with particular emphasis on low-power applications.

Despite the course taking the majority of the examples from the area of low power applications several techniques and design strategies presented are also widely used for high data rate transceivers.

The course starts with an overview of the main tasks of a wireless transceiver. After that the metrics to characterize the different properties of the RF front-end are discussed. By following a top-down structure the course will discuss the frequency synthesizer architectures followed by the most established and promising transceivers architecture for low power applications. In the second part of the course the main building blocks will be discussed: LNA, Mixers, PA, Oscillators and Filters.

The short course will end with an insight of the most promising techniques for major power efficiency including the promising quantized analog signal processing.

**Course Duration: 16 hrs** 

Course Format: 8 Sessions (1 session/week) x 2 hrs/ea. (90 min of lecture + 30 min of Q&A)

Course Work: Optional weekly homework sheets will be posted & collected via email





## **Online Short-Course on Advanced Wireless Transceiver IC Design**

## **Course Programme**

All Lectures @ 20:00-22:00 WET (Western European Time) = Dublin Time

#### **Lecture #1 - Introduction to Wireless Transceivers**

5<sup>th</sup> October 2020

An overview of the main tasks of wireless receiver and transmitter: Amplification, Filtering, Signal Up/Down-conversion followed by the most important metrics for wireless transceiver characterization. In particular matching, NF, 1dBCP, IP2-IP3 phase noise, ACLR and efficiency.

## **Lecture #2 - Phase-Locked Loops**

12<sup>th</sup> October 2020

This lecture will give an overview of phase locked loops and frequency synthesis: main task of a PLL, typical architectures and design trade-offs. Analog and Digital.

#### **Lecture #3 - Wireless Transceivers Architectures**

**19<sup>th</sup> October 2020** 

Following the top-down philosophy of the course, the most interesting and promising-architecture present in literature for wireless RX and TX targeting low power applications will be discussed.

#### **Lecture #4 - Low-Noise Amplifiers**

26<sup>th</sup> October 2020

The most common current mode LNA topologies will be investigated and compared: inductive degenerated LNA, feedback common gate, noise cancelling.

## <u>Lecture #5 - Mixers</u> 2<sup>nd</sup> November 2020

The mixer is a key building block of the receiver. The topology adopted typically influence the design of the entire radio. Current-mode approach is nowadays one of the most common solution. Three different topologies will be analysed: active mixers, and passive mixer, self-oscillating mixers.

## <u>Lecture #6 - Base-Band Filters</u>

9<sup>th</sup> November 2020

Filtering is one of the most challenging operation performed by the transceivers. Different low-power topologies will be discussed such as gm-C, OPAMP RC and passive switched capacitors filters.

#### <u>Lecture #7 - Power Amplifier and Frequency Generation</u>

16<sup>th</sup> November 2020

Power amplifiers and oscillators will be discussed in this lecture. It will be shown how there is a very straightforward relationship between these two blocks which has led the literature to use the same classification based on transistor operating region from A to F.

### <u>Lecture #8 - Power efficiency in wireless transceivers</u>

23<sup>rd</sup> November 2020

The course will end with an insight of different techniques to obtain power efficiency in analog RF front-end. Several example will be discussed such as current re-use techniques, merging functionalities and quantized analog signal processing.







Antonio Liscidini received the Laurea (summa cum laude) and Ph.D. degrees in electrical engineering from the University of Pavia, Pavia, Italy, in 2002 and 2006, respectively.

He was a summer Intern with National Semiconductors, Santa Clara, CA, USA, in 2003, studying poly phase filters and CMOS low-noise amplifiers. From 2008 to 2012, he was an Assistant Professor with the University of Pavia and a

consultant with Marvell Semiconductors, Pavia, in the area of integrated circuit. In 2012, he moved to the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada, where he is currently an Associate professor. In 2019 he has become consultant for Huawei Technology Group in the area of RFIC for optical communication. His research interests are focused on analog mixed signal interfaces with particular emphasis on the implementations of transceivers and frequency synthesizers for wireless and wireline communication.

Dr. Liscidini was a recipient of the Best Student Paper Award at the IEEE 2005 Symposium on VLSI Circuits and co-recipient of the Best Invited Paper Award at the 2011 IEEE CICC and Best Student Paper Award at the 2018 IEEE ESSCIRC. He has served as an Associate Editor for the IEEE Transactions on Circuits and Systems II: Express Briefs (2008-2011) (2017- 2018) and as a Guest Editor for the IEEE Journal of Solid-State Circuits (2013) (2016) and Guest Editor of the IEEE RFIC Virtual Journal (2018). He has been member of the ISSCC TPC (2012- 2017), of the ESSCIRC TPC (2010-2018), and of the CICC TPC (2019-currently). Between 2016 and 2018, he has been a Distinguished Lecturer of the IEEE Solid-State Circuits Society.