Online Short-Course on "Analog IC Design in Nanoscale CMOS"

By Tony Chan Carusone

Dates: 7th/10th/14th/17th/21th/24th/28th/1st September/October 2021

Host: Live-Virtual Zoom Lectures Hosted by University of Limerick

Course Outline

The course addresses the design of high-performance analog circuits in nanoscale CMOS technologies that offer analog circuit designers both benefits and challenges.

With transistor performance increasing and their size decreasing, parasitics are increasingly predominant contributors to overall circuit performance. Low supply voltages favour simple analog subcircuits and make power supply integrity critical for first-time-right-silicon.

The course begins by reviewing the transistor short-channel-length characteristics that particularly impact analog design in nanoscale technologies. We then discuss basic analog amplifier circuits compatible with low supply voltages and nanoscale CMOS technologies.

Subsequent lectures cover references and regulators, clock distribution and dynamic analog circuits. The final two lectures consider the design of ADCs and common pitfalls when integrating complex analog IP in nanoscale technologies.

Each lecture includes analog design case studies in technologies including 28nm bulk CMOS, 28nm FD-SOI, and 16nm FinFET. There will also be a focus on step-by-step methodologies for high-quality power supply integrity, low-jitter clock distribution, good layout practice, etc.

The course is intended primarily for analog designers with some experience in traditional bulk-CMOS technologies who may or may not have experience with technologies below 30nm. We will assume no familiarity with these advanced technologies and introduce them in the first two lectures.

Duration: **16 hrs**

Format: **8 'Live-Virtual' Sessions (2 sessions/wk) x 2 hrs/ea. (90min lecture + 30min Q&A)**

Work: **Optional homework assignments with access to SIMetrix simulator arranged.**

For information/registration, please contact Hooman Reyhani: hooman.reyhani@ul.ie

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Course Programme

All Lectures @ (16:00-18:00 WET) = (17:00-19:00 CET)

(20:30-22:30 IST) = (11:00-13:00 EST) = (08:00-10:00 PST)

Lecture #1 - CMOS Device Scaling & Modeling — **7th Sept. 2021**

Device scaling, short-channel length effects, analog design on bulk CMOS technologies below 30nm.

Lecture #2 - Advanced CMOS Technologies: SOI & FinFET — **10th Sept. 2021**

Impact on transistor model parameters, analog FOM & layout strategies. Reliability effects.

Lecture #3 - Amplifier Design in Nanoscale CMOS — **14th Sept. 2021**

Design of current mirrors & amplifier circuits. Suitable OTA topologies for low supply-voltage.

Lecture #4 - References, Regulators & Power Integrity — **17th Sept. 2021**

Diff. reference circuits & voltage regulation. Power distribution in ICs. Power integrity analysis.

Lecture #5 - Nanoscale CMOS Clocking — **21st Sept. 2021**

Jitter sources, amplification & power-supply-induced jitter. CMOS buffering & clock distribution.

Lecture #6 - Dynamic Comparators & Amplifiers — **24th Sept. 2021**

Applications of dynamic amplifiers (as integrators) in high-speed receivers. Dynamic comparators.

Lecture #7 - ADC-Based Receivers in Nanoscale CMOS — **28th Sept. 2021**

High-speed ADCs: folding-flash, binary search & CT pipelined. Combatting mismatch & applications.

Lecture #8 - Real-Life Cautionary Tales — **1st Oct. 2021**

Common design & layout errors, integrating large designs, power & clock routing, non-working chips.

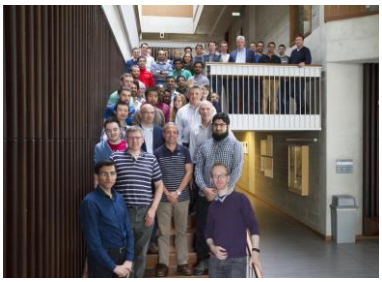
WET = Western European Time, CET = Central European Time,
IST = India Standard Time, EST = Eastern Standard Time, PST = Pacific Standard Time

Tony Chan Carusone (S'96–M'02–SM'08) received his Ph.D. from the University of Toronto in 2002 and has since been a professor with the Department of Electrical and Computer Engineering at the University of Toronto. He is also an occasional consultant to industry in the areas of integrated circuit design and digital communication.

Prof. Chan Carusone co-authored the Best Student Papers at the 2007, 2008 and 2011 Custom Integrated Circuits Conferences, the Best Invited Paper at the 2010 Custom Integrated Circuits Conference, the Best Paper at the 2005 Compound Semiconductor Integrated Circuits Symposium, and the Best Young Scientist Paper at the 2014 European Solid-State Circuits Conference. He co-authored the popular textbooks "Analog Integrated Circuit Design" (along with D. Johns and K. Martin) and "Microelectronic Circuits," 8th edition (along with A. Sedra, K.C. Smith and V. Gaudet). He was Editor-in-Chief of the IEEE Transactions on Circuits and Systems II: Express Briefs in 2009, an Associate Editor for the IEEE Journal of Solid-State Circuits 2010-2017 and is now Editor-in-Chief of the IEEE Solid-State Circuits Letters. He was a Distinguished Lecturer for the IEEE Solid-State Circuits Society 2015-2017 and currently serves on the Technical Program Committee of the International Solid-State Circuits Conference.

Past IC Design Courses Hosted by UL-CSRC

500+ participants from across the world: Austria, Belgium, Czech Rep., Germany, Italy, Spain, Portugal, Switzerland, Romania, Scotland, England, Ireland, India, Canada & US.



2015: Prof. Murmann

IEEE SSC Magazine - Winter 2016

2016: Prof. Murmann

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2017: Prof. Murmann

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2018: Prof. Bult

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2019: Prof. Johns

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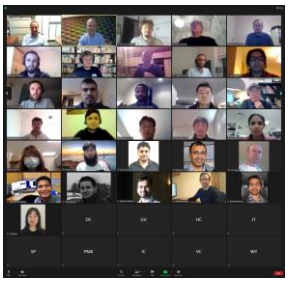
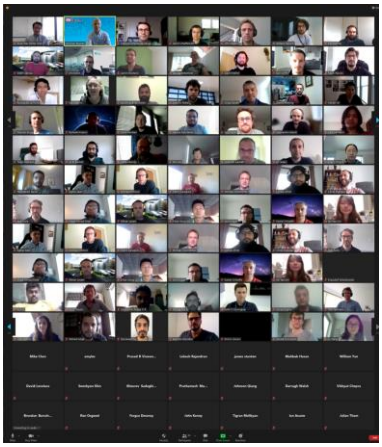


2020: Prof. Liscidini

IEEE SSC Magazine - Spring 2021



2021: Prof. Chen

IEEE SSC Magazine, Summer 2021

Past Participants From Industry & Academia