UNIVERSITY of LIMERICK
OLLSCOIL LUIMNIGH

csrc
circuits and systems research centre

2-Day Short-Course on Selected Topics in Mixed-Signal IC Design

By Klaas Bult

Date: 14th & 15th June 2018

Venue: University of Limerick

Power-Efficient Residue Amplifiers (based on AACD 2018 presentation) **2x1.5 hours**

Abstract: *A comprehensive method for power estimation of residue amplifiers is presented. Using this method a definition of power efficiency is given, which subsequently is used to analyze recently published, highly efficient residue amplifiers. Design parameters are identified which have a key influence on the power efficiency and design choices based on power efficiency are discussed. It is shown that the most power efficient residue amplifier topologies share the same core circuit and differ primarily in how this core circuit is driven from the input. Finally, an overview is given of these topologies, ranked on power efficiency.*

ADC Building Blocks (based on MEAD 2017) **1x1.5 hours**

Abstract: *Most ADCs are built from blocks like comparators, DACs, amplifier and logic. The operation and design of these blocks will be discussed. The core operation will be identified and based on that a fundamental estimate of their power dissipation will be given, based on specifications like dynamic range and sampling frequency. This will be used in the lecture on Energy Efficient Nyquist-Rate ADCs.*

Energy-Efficient Nyquist-Rate ADCs (based on ISSCC 2018 Forum) **2x1.5 hours**

Abstract: *In large SoC's Data Converters take a dominant position both from a performance point of view as well as from an energy consumption point of view. The past two decades have shown a strongly intensified search for more power efficient Data Converters, in particular power-efficient Analog-to-Digital converters. This presentation will focus on power efficiency of Nyquist-rate Analog to Digital converters and discuss what has been proposed in open literature to reduce the energy consumption, both from a circuit point of view as well as from an architectural point of view. To get a good grasp of how circuit and architectural choices affect the power consumption, a method will be introduced that allows a quick estimation of the power consumption of an ADC, based on the required SNDR, the sampling frequency, the used technology as well as the chosen ADC architecture and circuit implementations. The proposed method enables a comparison based on these choices and can show what their impact is on the power efficiency, without going through the elaborate design of several architectures. It also shows which recent inventions made a large impact on power efficiency and how these inventions can also be of use in other architectures than the ones they have been introduced in.*

Embedded ADCs (based on MEAD 2017) **1x1.5 hours**

Abstract: *Systems-on-Chip (SoCs) have been a reality in the past 15 years. Several dozens of different functional blocks are being integrated on a single die, reaching transistor counts of over a billion. From the Analog portion of an SoC the Data Converters are probably the most challenging blocks, often limiting system performance and dominating power dissipation. However, requirements regarding yield, die-size, scalability, noise immunity, power and the fact that logic is almost for free, cause distinct differences between embedded Data Converters and their stand-alone, usually general purpose, counterparts. The presentation describes these differences and provides an overview of the state-of-the-art in embedded Data Conversion.*

High-Speed CMOS DACs (based on MEAD 2017) **2x1.5 hours**

Abstract: *Introduction to high-speed current-steering DACs. The principle of current-steering DACs is extremely simple and a good designer needs to know all error mechanisms. Common error mechanisms will be discussed, with error sources affecting amplitude, timing or the shape of the basic output pulse. The problem of code-dependent output impedance is discussed, including solutions. A state-of-the-art DAC design will be shown, including measurements and comparisons to theory and literature.*

UNIVERSITY of LIMERICK
OLLSCOIL LUIMNIGH

csrc
circuits and systems research centre

Course Programme

Thursday, 14th June 2018

08:30-09:00	Registration & Welcoming
09:00-10:30	Lecture #1 - Power-Efficient Residue Amplifiers (Part I)
10:30-11:00	Coffee Break
11:00-12:30	Lecture #2 - Power-Efficient Residue Amplifiers (Part II)
12:30-13:30	Lunch Break
13:30-14:00	Guest Lecture (Arralis) - "FMCW Radar Design for Autonomous Vehicle"
14:00-15:30	Lecture #3 - ADC Building Blocks
15:30 -16:00	Coffee Break
16:00-17:30	Lecture #4 - Energy-Efficient Nyquist-Rate ADCs (Part I)

Friday, 15th June 2018

09:00-10:30	Lecture #5 - Energy-Efficient Nyquist-Rate ADCs (Part II)
10:30-11:00	Coffee Break
11:00-12:30	Lecture #6 - Embedded ADCs
12:30-13:30	Lunch Break
13:30-14:00	Guest Lecture (Jaguar Land Rover) - "Overview Automated Driving Systems"
14:00-15:30	Lecture #7 - High-Speed CMOS DACs (Part I)
15:30 -16:00	Coffee Break
16:00-17:30	Lecture #8 - High-Speed CMOS DACs (Part II)

Prof. Klaas Bult

Klaas Bult received an MSc. and a PhD. degree from Twente University in 1984 and 1988 respectively. From 1988 to 1994 he worked as a Research Scientist at Philips Research Labs, where he worked on Analog CMOS Building Blocks, mainly for application in Video and Audio Systems. In 1993-1994 he was also a part-time professor at Twente University. From 1994 to 1996 he was an associate professor at UCLA, where he worked on Analog and RF Circuits for Mixed-Signal Applications. In the same period he was also a consultant with Broadcom Corporation, in Los Angeles, CA and later in Irvine, CA, during which he started the Analog Design Group at Broadcom. In 1996 he joined Broadcom full-time as a Director, responsible for Analog and RF Circuits for embedded applications in broadband communication systems. In 1999 he became a Sr. Director and started Broadcom's Design Center in Bunnik, The Netherlands. In 2005 he was appointed Vice President and CTO of Central Engineering. As of 2016 he's an independent consultant Analog IC Design, operating from The Netherlands.

Klaas Bult is an author of more than 60 international publications and holds more than 60 issued US patents. He is a Broadcom Fellow, an IEEE Fellow, was awarded the Lewis Winner Award for outstanding conference paper on ISSCC 1990, 1992 and 1997, was co-recipient of the Jan Van Vessem best European Paper Award at ISSCC 2004 and the Distinguished paper Award of ISSCC 2014. He was also awarded the ISSCC Best Evening Panel Award in 1997 and 2006 and the Best Forum Speaker Award at ISSCC 2011. Klaas Bult has served more than 12 years on the ISSCC Technical Program Committee, 18 years on the ESSCIRC Technical Program Committee and 7 years as a member of the ESSCIRC/ESSDERC Steering Committee.

UNIVERSITY of LIMERICK
OLLSCOIL LUIMNIGH

csrc
circuits and systems research centre

Mr. Yulung Tang

Yulung Tang received a BSEE and a MS Graduate Inst. Of Communication Engineering degree from National Taiwan University in 1998 and 2000 respectively. In 2014 he received a MSEE degree from California Inst. of Tech, Pasadena, USA.

Yulung moved to Ireland in March 2017 to take up the role as Senior MMIC Design Engineer at Arralis. In this role, he mainly works on System and MMIC development for mmW FMCW/phased-array radar and satellite communication front-end. Prior to Arralis, Yulung worked at ETS-Lindgren as Asia RF Engineering Manager in Taiwan, from 2008 to 2016. His job included designing EMC and antenna pattern measurement system, anechoic chamber designing and managing Asia engineering team. From 2005 to 2008, Yulung worked as a Design Engineer at TriQuint Semiconductor, where he developed PA MMIC and modules for mobile phones, in Oregon, USA. As a Research Assistant in Caltech from 2003 to 2004, he researched mmW technologies and developed cryogenic LNA for radio astronomy applications.

About Arralis: Arralis is a rapidly scaling company, providing world leading expertise in RF, micro and millimetre-wave technology. Arralis has offices in Ireland, UK, USA, Hong Kong and a fabrication facility in China. It's core focus is in W-, Ka- and E- bands, where it is building fully integrated RF front ends. Arralis designs and manufactures MMICs, modules and antennas for these bands and provide fully integrated systems for vision and radar applications.

Mr. Peter Barry

Peter Barry received BEng degree from University of Limerick in 1991.

As Chief Software Architect Autonomous Driving, Peter is a seasoned technical leader, with 27 years in development of distributed/embedded computing platforms. He currently leads the software team at Jaguar Landover with responsibility to bring Level 4 autonomy to Jaguar Landover's products.

Prior to this role, Peter was a Senior Principal Engineer at Intel, where he led the definition and development of numerous products such as Intel's in vehicle infotainment platforms and IoT Quark Product line. Peter has published two textbooks and holds 23 patents.