

# Real-World CMOS RF Transceivers Course

The [“CMOS RF Transceivers - Challenges & Solutions”](#) online short-course, held in September 2023, attracted a worldwide participation of 100 analog design engineers and research students from 23 countries, across 5 continents and 19 time-zones, where Prof. Thomas Byunghak Cho (KAIST) kindly shared his deep understanding of RF circuits and systems design as well as invaluable practical considerations for product design. There was tremendous Q&A participation during the online sessions with additional Q&A on the offline discussion forums.

The countries represented at this intercontinental course were: Japan, China, S. Korea, Singapore, India, Israel, Egypt, Greece, Italy, Austria, Germany, Poland, Sweden, Belgium, Netherlands, Switzerland, Portugal, England, Scotland, Ireland, Canada, USA and Brazil.

The course provided a comprehensive overview of CMOS RF transceiver design, ranging from relevant signal processing concepts to real-world case studies, identifying the design challenges and the discussion of circuit and system solutions when designing practical CMOS RF transceivers.

The main topics included: Review of basic signal processing concepts; Evolution of CMOS RF transceiver architectures; Transceiver design deep-dive; Rx & Tx key specification, understanding and system performance; Practical design consideration; Multi-band Receiver (Case Study); IoT SoC (Case Study); FR2 Chipset (Case Study); Future challenges.

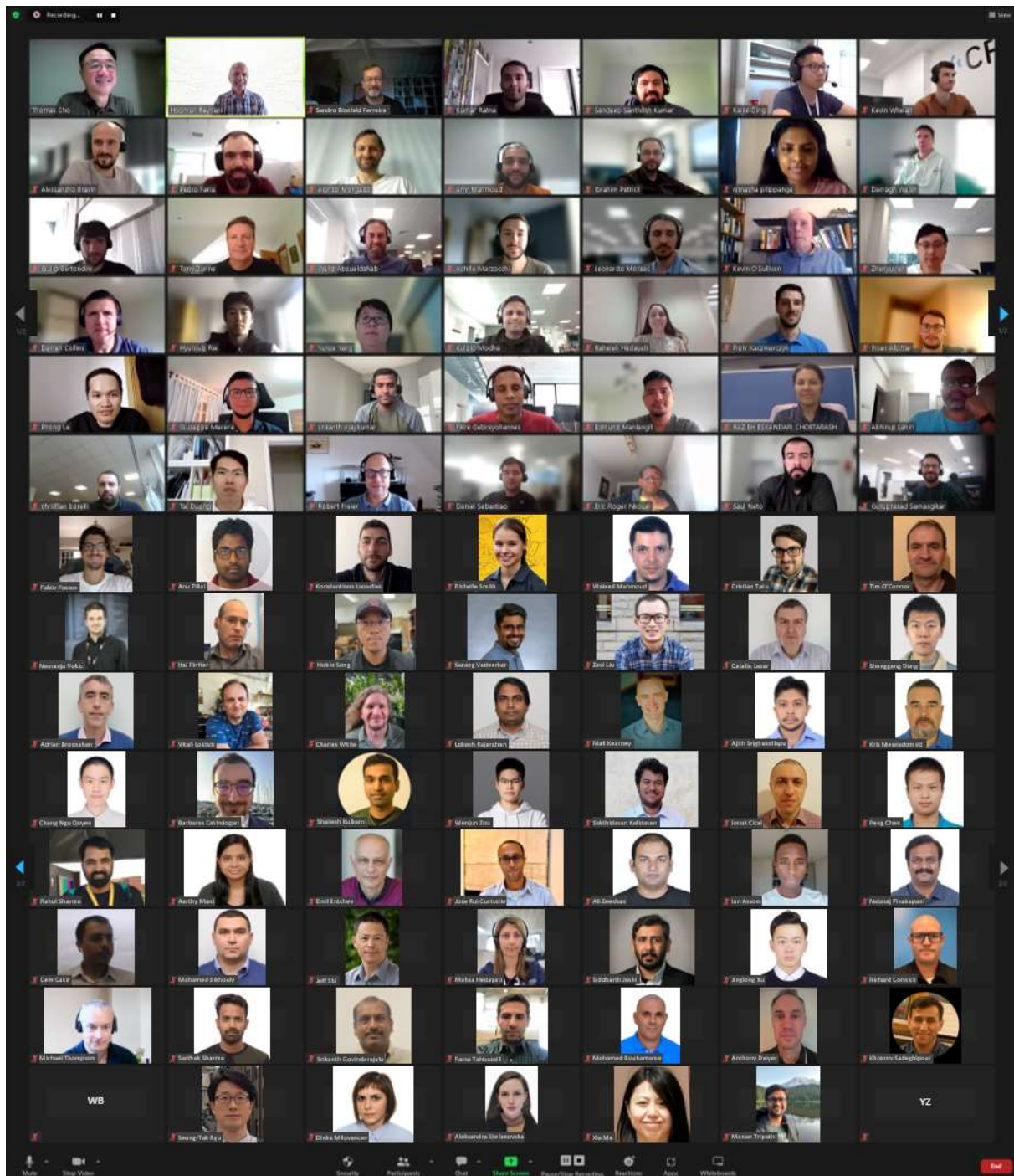
The screenshot shows a presentation slide titled "CMOS Power Amplifier Architecture". On the left is a circuit diagram of a two-stage CMOS PA. The top stage is a drive stage with a PMOS transistor (PVBB) and an NMOS transistor (Vcg2). The bottom stage is a power stage with a PMOS transistor (VDD) and an NMOS transistor (Vcg1). An Adaptive Biasing (ADB) block is connected between the two stages, receiving feedback from the output (RF<sub>out</sub>) and providing biasing (Vcs2) to the drive stage. The input is RF<sub>in</sub> and the output is RF<sub>out</sub>. Handwritten blue annotations include "23dBm" near the output, "Configured Two stages" with arrows pointing to the two transistor stages, "Adaptive biasing (ADB) for PA linearity improvement" with a circle around the ADB block, and "Power-cell slicing for PA efficiency improvement" with a circle around the NMOS transistor in the power stage. To the right of the diagram is a graph of output power (P<sub>out</sub>) versus input power (P<sub>in</sub>) showing a linear region and a compression region. A small video inset in the bottom right corner shows Prof. Thomas Byunghak Cho speaking.

**CMOS Power Amplifier Architecture**

- **23dBm transmitting output power**
- **Configured Two stages**
  - High voltage gain in a drive stage
  - Required power gain in a power stage
- **Adaptive biasing (ADB) for PA linearity improvement**
  - Consisting of an attenuator, a power detector, an operational amplifier
- **Power-cell slicing for PA efficiency improvement**

Prof. Thomas Byunghak Cho (KAIST), course presenter, talked about **“CMOS RF Transceivers”** at an online course hosted by Hooman Reyhani, Ireland.

Prof. Cho is currently an Invited Professor at the School of Electrical Engineering at the Korea Advanced Institute of Science and Technology (KAIST) in S. Korea. He was previously with Level One (USA) and Wireless Interface (USA). In 2004 he joined Marvell Semiconductor (USA) and in 2012 Samsung Electronics (S. Korea). His technical interests include RF/analog/mixed-signal circuit design for wireless/wireline communication and analog-to-digital interface circuits for sensor applications. Dr. Cho has authored or co-authored over 40 journal articles and conference papers and holds more than 40 patents. He is an IEEE Fellow.



The lecturer, organizer and many of the participants of the **"CMOS RF Transceivers – Challenges & Solutions"** online course, September 2023.

The feedback from the course participants was very positive. One participant wrote, *"High quality in all aspects, from the professor engagement & delivery, to the course material, homework assignments and the overall course organization"*. Another said, *"Case studies build well on the material (from first half of the course) and show the practical considerations and trade-offs when designing for a real application"*. While another commented, *"Sessions being recorded means it can be played back and paused. This enhances the learning outcome for me. It also means that I can catch up if I miss a lecture due to work commitments"*.

Full access to this course content, as well as our previous courses, may be requested (subject to payment) via [here](#). For more information, [please see here](#).

— Hooman Reyhani