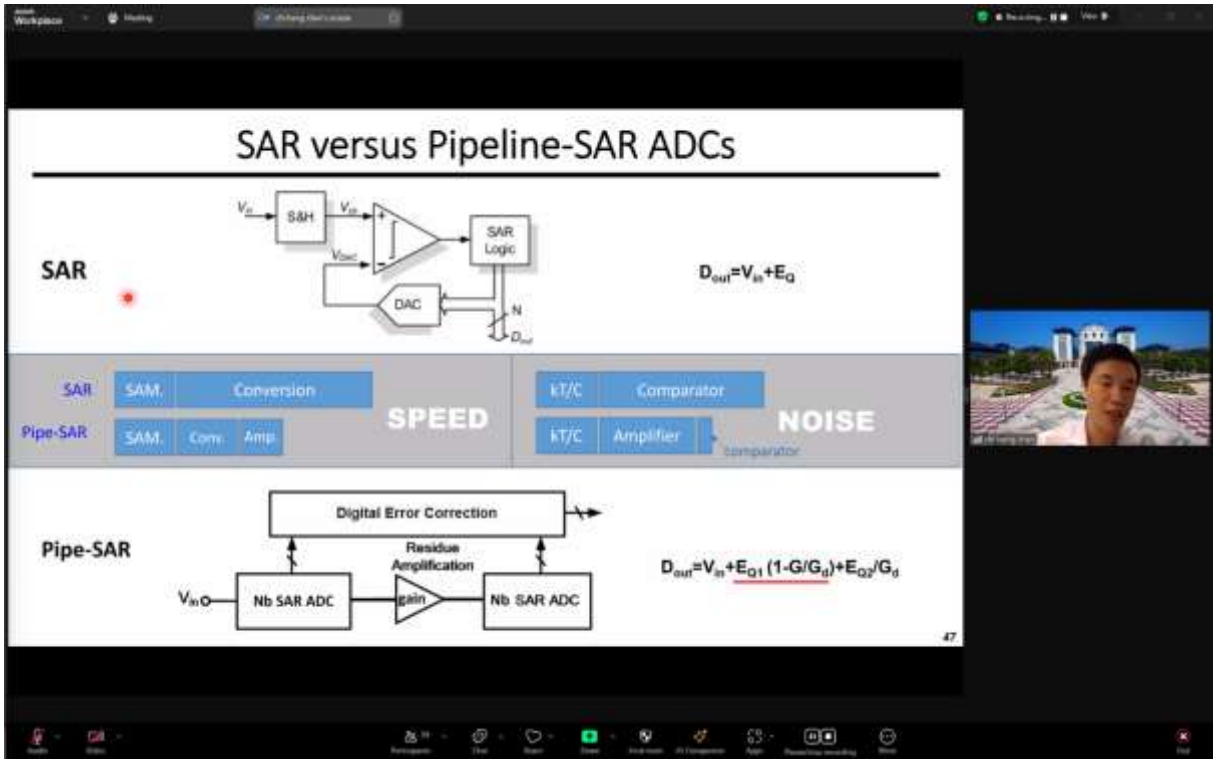
SAR ADC Course Celebrates Special Milestone

Time-Interleaved (TI) Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs) have evolved considerably since the first ever reported 6-bit 600MSPS TI SAR ADC implementation on 90nm Digital CMOS at ISSCC 2004. Over the past two decades SAR ADCs have continuously broken performance barriers and become the most energy-efficient ADC topology at low-medium resolutions. Significant improvement in Signal-to-Noise-Distortion (SNDR) performance has been reported by adoption of calibration and digital error correction techniques to overcome channel-to-channel non-idealities in TI implementations. The hybrid combination of SAR and Pipeline topologies are being used to optimize speed, Effective-Number-Of-Bits (ENOBs) and power dissipation even further. Nanoscale technologies have paved the way for small-area TI SAR ADCs to achieve sampling rates beyond 100GSPS as part of large System-on-Chip (SoC) integration. The ever-increasing appetite for higher data-rates, from communication to automotive to industrial to healthcare to cloud computing and AI, is the driving force behind the continued research and development of multi-GSPS SAR-type ADCs at extended resolutions.

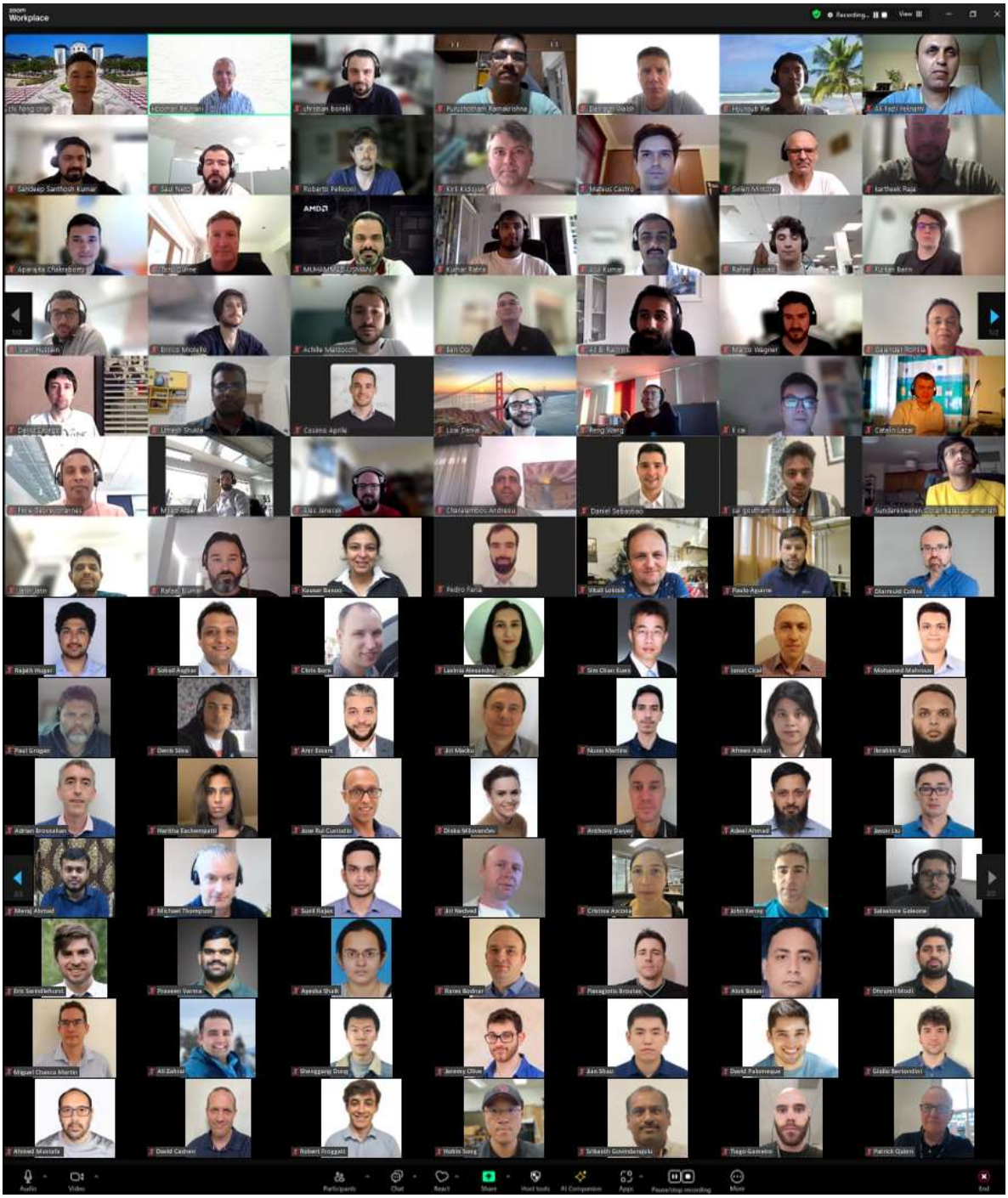
The ***"Extreme SAR ADCs – Exploring New Frontiers"*** online course, held in May 2024, celebrated twenty years of remarkable SAR ADC architecture innovations and circuit design techniques by providing an in-depth walkthrough from theoretical to practical considerations on extreme speed SAR ADCs. The 120 participants, from industry and academia, were guided by Prof. Chi-Hang Chan (University of Macau), from fundamental concepts to state-of-the-art implementations followed by practical case studies, continuously exploring new frontiers to extend present day performance.



Prof. Chi-Hang Chan (University of Macau), course presenter, talked about ***"Extreme SAR ADCs"*** at an online course hosted by Hooman Reyhani, Ireland.

The 28 countries represented at this international course were: Japan, Taiwan, S. Korea, Singapore, India, Türkiye, Israel, Egypt, Cyprus, Greece, Italy, Romania, Austria, Germany, Switzerland, Czechia, Poland, Sweden, Belgium, France, Spain, Portugal, England, Scotland, Ireland, Canada, USA and Brazil.

The main topics included: Massive Time-Interleaved SAR ADCs; Input Buffer & Reference Buffer; Extreme Samplers & Comparators; Clocking & Extreme Amplifier; High-Speed SAR ADCs; Pipeline-SAR ADCs; Digitally-Assisted TI SAR ADCs; ADC Design, Layout & Verification.



The lecturer, organizer and the participants of the ***"Extreme SAR ADCs – Exploring New Frontiers"*** online course, May 2024.

Prof. Chan is currently an Associate Professor at the University of Macau, Macao, China, where he leads a large research team, working on various types of ADCs, PLLs, Smart Time-of-Flight and AI. His research interests include high-speed Nyquist, wideband oversampling ADCs, ADC calibrations, ring oscillator-based PLLs, and mixed-signal circuits. Dr. Chan has published over 100 peer-reviewed papers, including 18 ISSCC papers, 22 JSSC papers, 26 Solid-State conference and VLSI conference papers between 2011-2024. He is a multi-award winner, including SSCS Pre-doctoral Achievement Award, 2015. He serves as a data converter subcommittee TPC member of IEEE A-SSCC.

The overall feedback from the course participants was extremely positive:

"Best course ever, really nice and expert person. Very up to date content. Clearly presented."

"Unlike some ADC courses, Prof. Chan has focused on some of the overlooked elements of ADC design like buffering and clock constraints. Slides and presentation were very clear and crisp."

"Fantastic course content and format. Homework assignments were quite helpful. Would highly recommend your courses."

Full access to this course content, as well as our previous courses, may be requested (subject to payment) via here. For more information, please see here.

— Hooman Reyhani