

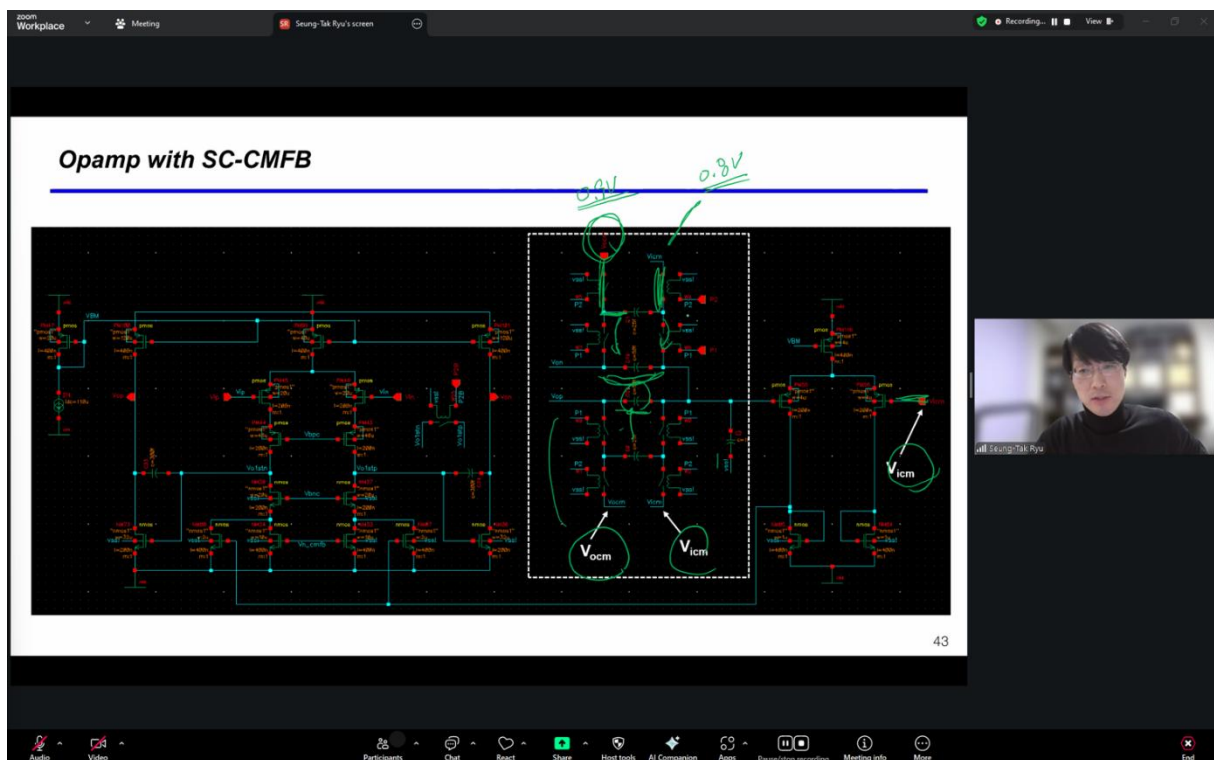
# Intuition-Driven Analog IC Design Course for Modern Engineers

Building on the formidable momentum of our 2025 sell-out courses, the January 2026 online course, [\*\*\*“Analog IC Design – Essential Insights”\*\*\*](#), drew a global audience of 100 participants, representing semiconductor technology giants and leading research organisations, under the guidance of Prof. Seung-Tak Ryu (KAIST), an award winning educator in analog and mixed-signal IC design.

The course focused on the cultivation of “Engineering Intuition”, challenging the prevailing brute-force simulation culture. This structured, practical exploration was centred on the operational amplifier (opamp) as a fundamental building block encompassing the most essential design challenges, including gain, bandwidth, feedback, stability, frequency and transient response, noise, and matching. The curriculum bridged the gap between foundational opamp principles and sophisticated Switched-Capacitor (SC) techniques, equipping the attendees to transition seamlessly from theoretical concepts to silicon-ready implementations.

The participants joined this international gathering from a total of 19 countries, including: Hong Kong, Vietnam, Singapore, India, Italy, Austria, Switzerland, Poland, Belgium, Netherlands, Spain, Portugal, England, Scotland, Ireland, Canada, United States, Brazil, and Argentina.

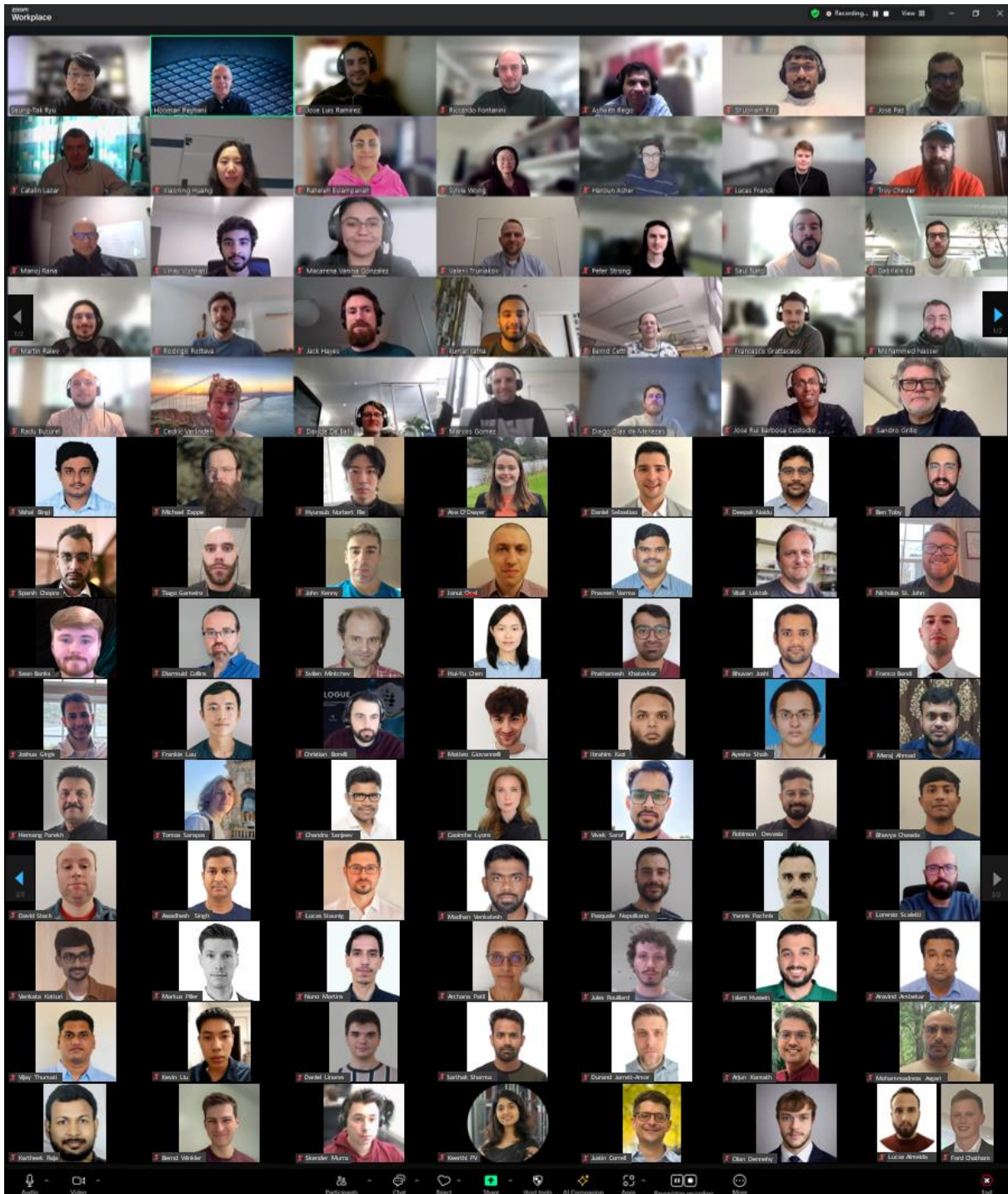
The curriculum roadmap evolved across Opamp Fundamentals, Simple and Two-Stage Opamps, and Miller Compensation, through to Transient Response and High-Gain architectures. The progression then moved into Fully-Differential Opamps and Advanced SC Amplifiers, concluding with sophisticated SC Gain Amp design.



The image is a screenshot of a Zoom meeting. The main content is a slide titled "Opamp with SC-CMFB". The slide features a complex circuit diagram of an operational amplifier with a switched-capacitor common-mode feedback (SC-CMFB) stage. The diagram is annotated with green handwritten notes: "0.8V" and "0.8V" at the top, and "V<sub>ocm</sub>" and "V<sub>icm</sub>" at the bottom. A dashed white box highlights a central portion of the circuit. The slide number "43" is visible in the bottom right corner. In the bottom right corner of the Zoom window, there is a video feed of Prof. Seung-Tak Ryu, who is wearing glasses and a dark shirt. The Zoom interface includes a top bar with "Meeting" and "Seung-Tak Ryu's screen" and a bottom toolbar with icons for Audio, Video, Participants, Chat, React, Share, Host tools, AI Companion, Apps, Presentation recording, Meeting info, and More.

Prof. Seung-Tak Ryu (KAIST), presented ***“Analog IC Design – Essential Insights”***, at an online course hosted by Hooman Reyhani, Ireland.

Prof. Seung-Tak Ryu has been a faculty member in the Department of Electrical Engineering at KAIST (Korea Advanced Institute of Science and Technology) since 2009. A leading expert in analog and mixed-signal IC design, his research focuses particularly on data converters, with an impressive portfolio of 130+ research publications and 48 patents. Dr. Ryu is a TPC member for ISSCC, ASSCC and ESSCIRC and currently serves as an Associate Editor for OJ-CAS and OJ-SSCS. He served as a Distinguished Lecturer for the IEEE SSCS, 2021-2022.



The lecturer, organiser and participants of the *“Analog IC Design – Essential Insights”* online course, January 2026.

The course featured two intensive hands-on design projects. Project #1 guided participants through a rigorous design methodology, moving from initial specifications to final circuit simulations, for a fully-differential two-stage opamp. Incorporating Continuous-Time CMFB for a 2.8b/stage MDAC within a 10b 50MS/s Pipelined ADC, the project was implemented on a 180nm technology node.

**Design Project #1**

- Target: Design a fully-diff two-stage opamp with CT CMFB for 2.8b/stage MDAC (10b 50MS/s Pipelined ADC)
- Technology: 180nm
- Supply Voltage = 1.8V
- MDAC unit cap = 250fF
- MDAC load cap = 1pF
- Opamp loop-gain (with a feedback factor of 1/5) > 60dB
- Feedback factor of 1/5 allows for parasitic capacitance
- Opamp unity loop-gain BW (with a feedback factor of 1/5) > 120MHz
- Phase margin > 60deg
- MDAC input & output voltage swing (single-ended): 0.4V - 1.4V at  $V_{ocm} = 0.9V$
- Opamp input common level: can be fixed to a certain DC level (bottom plate sampling)
- Bias circuit to be designed as well
- Consider settling accuracy of the target MDAC (including slew rate)
- Power consumption: as low as possible

**Design Project #1**

10b 50MS/s Pipelined ADC

Design Project #1: Target Specifications

Project #2 provided a unique and valuable learning opportunity by exploring the complexities of design failure. When an initial attempt to design a Ringamp for a 10b 200MS/s Pipelined ADC MDAC fell short of the aggressive target specifications, Prof. Ryu provided a detailed analysis of the performance bottlenecks. To ensure a comprehensive understanding, an additional lecture was arranged to walk through a successful design solution tailored to revised specifications for a 10b 50MS/s Pipelined ADC.

**Design Project #2**

- Target: Design a Ringamp for 2.8b/stage MDAC (for 10b 50MS/s Pipelined ADC)
- Technology: 180nm
- Supply Voltage = 1.8V
- MDAC unit cap = 250fF
- MDAC load cap = 1pF
- Opamp DC loop-gain (with a feedback factor of 1/5) > 48dB
- Feedback factor of 1/5 allows for parasitic capacitance
- MDAC input & output voltage swing (single-ended): 0.3V - 1.5V at  $V_{ocm} = 0.9V$
- SFDR for full range swing > 60dB
- Opamp input common level: can be fixed to a certain DC level (bottom plate sampling)
- Bias circuit to be designed as well
- Power consumption: as low as possible

**Design Project #2**

10b 50MS/s Pipelined ADC

Design Project #2: Revised Target Specifications

The [course preview video](#), a short [lecture extract video](#), and a [sample homework assignment video](#), highlight the material presented throughout this training course.

Representative feedback:

*“Very well presented. Practical projects & solutions. I’d recommend this course to anybody in the field.”*

*“I like there is the facility to catch-up and/or review course material and lectures asynchronously.”*

Full access to [this course content](#), as well as [previous courses](#), may be requested (subject to payment). For more information, [please visit our online portal](#).

— Hooman Reyhani