

Eight IC Design Icons Unite for Eight Masterclasses

The May 2026 online course, [*"ICONS 2026: Masterclass Series on Advanced IC Design"*](#), departed from our established course format centred on a single specialist topic and lecturer, bringing together eight leading experts from academia and industry for a new series of deep-dive masterclasses spanning some of the most demanding challenges in modern analog and mixed-signal IC design. The masterclasses were designed around a two-part teaching approach, progressing from the engineering "why" in the first part to the practical "how" through design and implementation in the second.

The technical programme spanned Data Conversion, Frequency Synthesis, Wireline Transceivers and Advanced Measurement, covering sampling circuits, advanced ADC architectures, PLLs, high-speed SerDes, oscillators and measurement techniques, with an emphasis on systematic design methodologies and engineering insight.

The eight masterclasses were presented by [Boris Murmann](#) (University of Hawai'i), [Seung-Tak Ryu](#) (KAIST), [Chi-Hang Chan](#) (University of Macau), [Woogeun Rhee](#) (Sungkyunkwan University), [Gain Kim](#) (DGIST), [Kevin Zheng](#) (AMD/Xilinx), [Antonio Liscidini](#) (University of Toronto), and [Shahriar Shahramian](#) (Nokia Bell Labs).

The course was attended by 100 design engineers and research graduates from 25 countries across five continents: Japan, S. Korea, China, Taiwan, Vietnam, Singapore, India, Türkiye, Egypt, Israel, Italy, Austria, Czechia, Germany, Poland, Switzerland, Netherlands, Belgium, Spain, Portugal, England, Ireland, USA, Brazil and Argentina.

The screenshot displays a Zoom meeting interface with four slides visible in a 2x2 grid. The top-left slide, titled 'Testbench', shows a circuit diagram of an 'Ideal flip-around circuit' with a 'Bootstrapped switch' and 'Clocking' signals. The top-right slide, titled 'Step1: 3rd Stage Sizing: Slew Simulation with Step Input', shows a 'Slew simulation result' with waveforms for 'FIA1 (t_{on})', 'FIA2 (t_{on})', and 'FIA3 (t_{on})'. The bottom-left slide, titled 'Constant-Slope or Fixed-Slope VTC', shows a 'Discharging-based VTC' circuit diagram and a 'Crossing Detector' block. The bottom-right slide, titled '<0.5V 2.4GHz ΔΣ HPLL with Voltage-Mode PI', shows a block diagram of the HPLL and plots for 'Measured Phase Noise' and 'Measured Spur'. The Zoom interface includes a 'Meeting' window at the top, a 'Participants' list on the left, and a 'More' menu at the bottom right.

Boris Murmann, Seung-Tak Ryu, Chi-Hang Chan and Woogeun Rhee presented Lectures #1 to #4 of *"ICONS 2026: Masterclass Series on Advanced IC Design"*, hosted by Hooman Reyhani, Ireland.

The Data Conversion masterclasses began with Boris Murmann's systematic approach to sampling-circuit design for ultra-high-speed and ultra-low-distortion applications, progressing from specifications and fundamental limitations to transistor-level implementation and simulation. Seung-Tak Ryu explored residue-amplifier design methodologies for pipelined ADCs, including dynamic Ringamp and Floating Inverter Amplifier (FIA) techniques, while Chi-Hang Chan presented Time-Domain ADCs, taking participants from fundamental concepts and architectures through transistor-level implementation to PVT-robust verification.

Frequency Synthesis was addressed by Woogeun Rhee, who explored Hybrid PLLs with Linear Phase Detection as a technology-scalable alternative to conventional all-digital approaches. Antonio Liscidini examined Harmonic LC Oscillators, highlighting fundamental limits and design trade-offs involving phase noise, power efficiency, tunability and device noise.

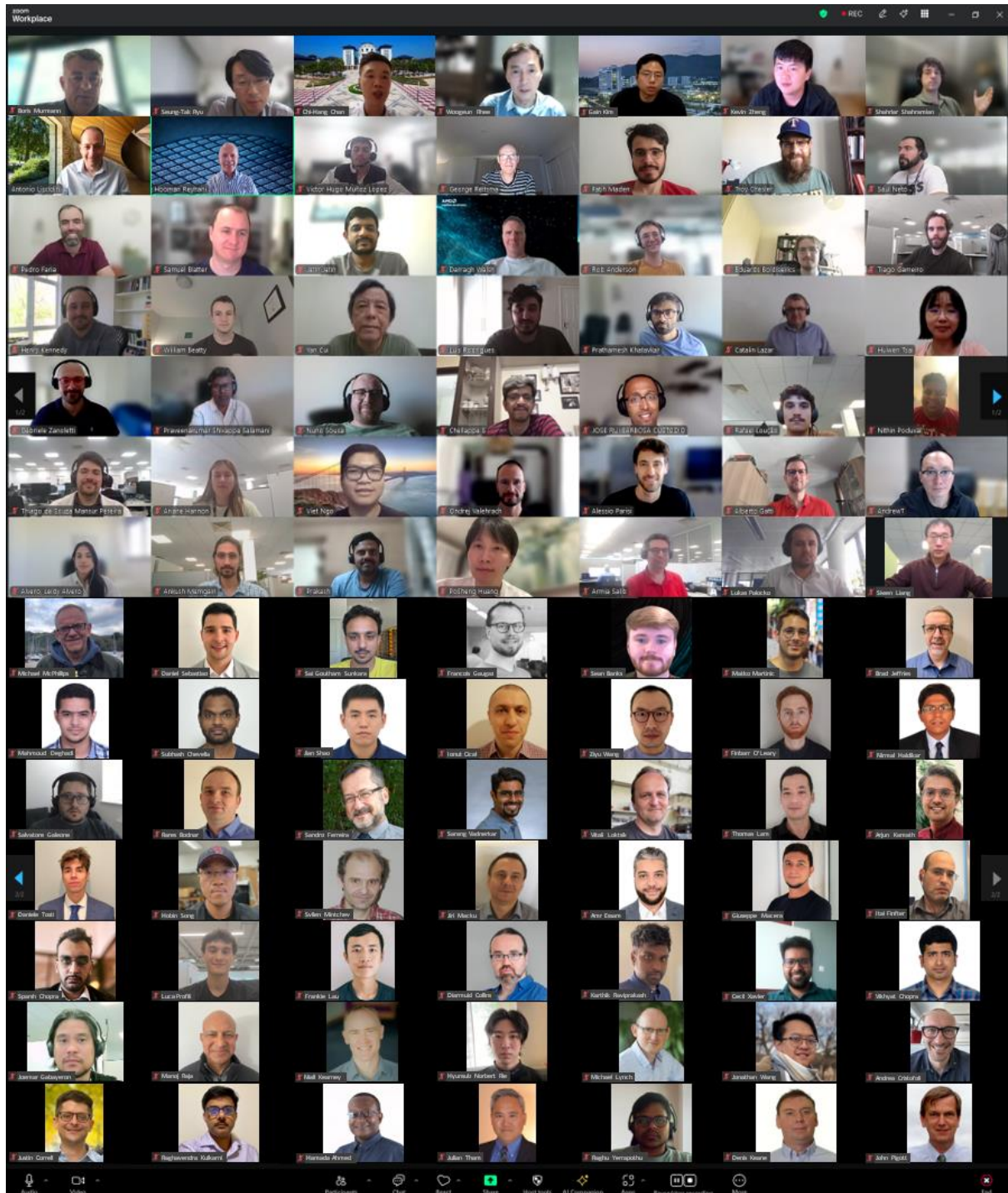
The Wireline Transceiver masterclasses combined circuit- and system-level perspectives. Gain Kim presented a step-by-step CTLE design methodology for high-speed PAM-4 receivers, progressing from system specifications to transistor sizing and passive-component selection, while Kevin Zheng explored system and circuit modelling for modern SerDes links, including equalisation, clock and data recovery, jitter and noise.

Completing the series, Shahriar Shahramian explored advanced measurement techniques and common pitfalls across frequency-, time- and mixed-domain characterisation, ranging from noise figure, phase noise and broadband modulation to eye diagrams and sub-THz signal detection. The masterclass also examined the practical limits of instrumentation and the importance of measurement uncertainty, repeatability and robust fault detection.

The screenshot displays a Zoom meeting interface with four slides visible in a grid. The top-left slide, titled 'Practical CTLE With Finite r_o and Inductive (L) Peaking', shows circuit diagrams and plots of magnitude and phase response. The top-right slide, 'Wireline links in a nutshell', illustrates a block diagram of a TX channel RX system with waveforms for correct and distorted signals. The bottom-left slide, 'Summary preliminary sizing (Virtuoso 65nm)', presents a circuit schematic and a list of design considerations for a 2mA current source. The bottom-right slide, 'Eye Diagram Capture Considerations', shows eye diagrams and discusses the impact of insufficient sampling counts. The Zoom interface includes a top bar with 'Zoom Workplace' and 'Meeting' tabs, and a bottom bar with various controls like 'Participants', 'Chat', and 'Share'.

Gain Kim, Kevin Zheng, Antonio Liscidini and Shahriar Shahramian presented Lectures #5 to #8 of “**ICONS 2026: Masterclass Series on Advanced IC Design**”, hosted by Hooman Reyhani, Ireland.

Beyond the breadth of technical content, ICONS 2026 offered participants eight different perspectives on advanced IC design, from fundamental understanding and circuit implementation to system modelling and measurement. The complementary expertise of the presenters, reinforced by interaction and technical discussions throughout the live sessions, exposed participants to contrasting approaches to analysing, designing, modelling and measuring advanced integrated circuits.



The eight presenters, organiser and participants of the *“ICONS 2026: Masterclass Series on Advanced IC Design”* online course, May 2026.

Participants received comprehensive lecture notes, video-on-demand recordings, recommended reading and supplementary material, allowing them to revisit technically demanding topics at their own pace. Optional homework assignments provided opportunities to apply concepts introduced during the masterclasses through analytical exercises, circuit simulation and system-level modelling. The class discussion forum supported further technical exchange and offline Q&A throughout the course.

Course preview videos ([L1](#), [L2](#), [L3](#), [L4](#) and [L5](#)), a short [lecture extract](#) and sample homework assignment videos ([HW1](#) and [HW5](#)) offer a glimpse into the technical content, teaching approach and practical orientation of ICONS 2026.

Encouraging feedback began arriving even before the first live masterclass. After reviewing the Lecture #1 notes, one participant commented:

"I went through the Lecture #1 notes, and they're excellent. The step-by-step progression from theory to idealized schematics to real simulations is particularly effective".

Feedback collected at the end of the four-week series echoed this emphasis on combining theoretical understanding with hands-on design, while also highlighting systematic design methodologies and industry relevance.

One participant particularly valued the intended two-part format combining theory with hands-on design, describing the combination as *"highly valuable and rare to see"*. Another praised the *"hands-on approach of teaching"* and the opportunity to learn or refine a design methodology, while a third summarised the industry connection simply: *"The best part is how industry relevant the coursework is to what we use in industry"*.

Full access to [ICONS 2026](#), as well as [previous courses](#), may be requested (subject to payment). Further information is available through [our online portal](#).

— Hooman Reyhani